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AN11303

Integrated Common Mode Filter with ESD protection

Rev. 1 — 8 May 2014 Application note

Document information

Info	Content
Keywords	Common Mode Filter, CMF, differential signals, LVDS, ESD protection, EMI filter, USB, MIPI, D-PHY, CSI, DSI
Abstract	This document provides an overview about common mode filters with integrated ESD protection for USB 2.0 and the MIPI D-PHY interfaces.

Revision history

Rev	Date	Description
AN11303 v.1	20140508	Initial version

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1. Common Mode Filter for Low-Voltage Differential Signal Lines

1.1 Introduction

During the past two decades typical data rates on various electrical interfaces in computing and communication applications continuously increased. At the same time reduced power consumption and improved EMI robustness became more important. This process is still ongoing. Today many parallel interfaces are obsolete and have been replaced by serial high-speed differential interfaces:

External interfaces:

- LPT printer port → USB interface
- SCSI → eSATA, Firewire, Thunderbolt
- VGA → DVI, HDMI, Displayport

Internal interfaces:

- IDE / PATA → SATA
- ISA, PCI → PCIe
- Parallel camera interface → MIPI Camera Serial Interface (CSI)
- Parallel display interface → MIPI Display Serial Interface (DSI)

1.1.1 Advantages of low-voltage differential signal lines

High-speed aspects

With the miniaturization of modern CMOS processes supply voltages and logic levels are reduced from one evolutionary step to another. Power consumption could be reduced and operation time of battery driven applications (mobile phones, tablet PCs, personal navigation systems) could be increased. Lower signal voltages also reduce the unwanted RF emission raised from any high-speed data line.

Differential signals allow a better utilization of the complete level range: Transmitter and receiver in ground referenced systems typically define a maximum LOW level and a minimum HIGH level with an undefined (and thus unused) level range in between.

The receiver for a differential signal considers the difference between both signal lines and derives from the polarity of this difference the logical LOW or HIGH level. As a consequence the complete available level range is utilized for maximum robustness against noise.

EMI / EMC aspects

Since differential signals are transmitted on balanced symmetrical lines the transmission is isolated from any ground reference. The mechanism of galvanic coupling (ground bounce) between different signals is eliminated.

In a differential signal transmission the currents through the two conductors have opposite polarity. Likewise the actual voltage on each line is opposite, which keeps the magnetic and electric field concentrated between the two conductors. Finally the field strength in a moderate distance is very small as the opposite field components cancel each other. On

the one hand this factor keeps any unwanted radiation – i.e. electromagnetic emission – to a low level. On the other hand the transmission line itself is less susceptive against unwanted RF signals from other components or systems.

Cost aspects

The use of few differential lines in order to replace a larger number of parallel signals allows the reduction of external pins for integrated circuits as well as for connectors. In combination with reduced PCB area for signal routing a significant size reduction of a complete application is achievable.

A comparison of old computer main boards with ISA or PCI bus systems against new PCIe systems makes it very obvious. In the same way internal interfaces in portable equipment have been replaced allowing significant size reduction.

2. Common Mode Filter for USB 2.0 interfaces

2.1 EMI of USB 2.0 in mobile phones

Almost every smartphone is equipped with a USB 2.0 interface which allows the connection to PCs for data exchange and the charging of batteries. Many phones also support the USB On-The-Go (OTG) functionality which allow the phones to act as USB hosts in order to attach USB devices like a keyboard, a flash drive, a printer or other peripheral equipment.

The nominal data rate in high-speed mode according to the USB 2.0 specification is 480 Mbit/s. The major part of the spectral power density is located below 480 MHz. Still significant power is present around 960 MHz. Related to its clock frequency the USB interface itself is a potential source of disturbance for the GSM receiver in a phone. The GSM-900 systems (P-GSM-900, E-GSM-900, R-GSM-900) include the spectrum up to 960 MHz in their respective downlink bands.

As depicted in Figure 1, there are two possible scenarios for unwanted ElectroMagnetic Interference (EMI): The external USB cable is suited to radiate common mode noise caused by the digital USB circuits. All spectral components that match the receiver frequency are likely to degrade the sensitivity of the GSM or 3G reception. In a reciprocal manner the high transmit power of the GSM transmitter could disturb the USB data transmission and increase the Bit Error Rate (BER).

The best element to isolate the differential USB data transmission from the radiated GSM transmission is the application of common mode filters. Ideally these filters do not impair the transmission of the differential digital data, i.e. the insertion loss for the differential mode is small for the relevant spectrum. At the same time the Common Mode Rejection (CMR) of the filter blocks the unwanted radiation as well as the unwanted reception of external noise.

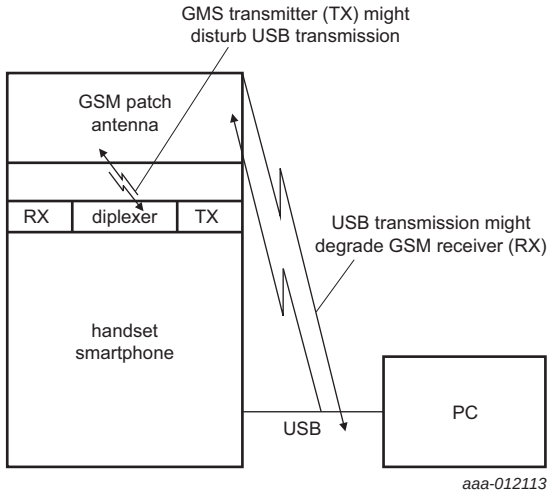


Fig 1. Potential ElectroMagnetic Interference (EMI) between GSM module and USB interface

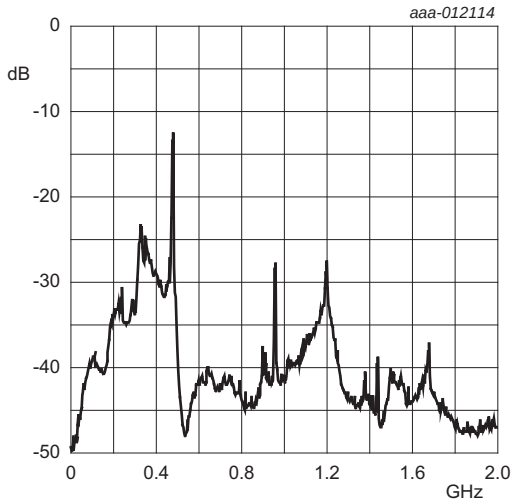
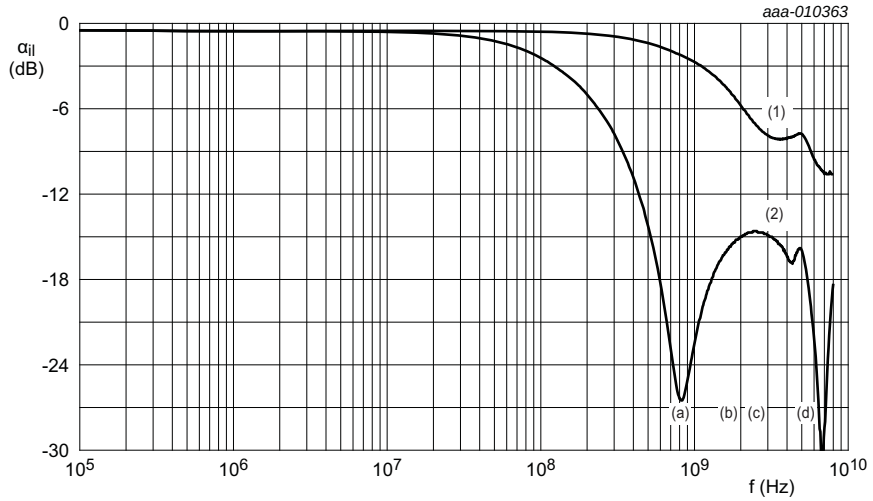


Fig 2. Measured spectrum of USB 2.0 data lines with continuous data traffic (high-speed mode, 480 Mbit/s)

2.2 Common Mode Filter with integrated ESD protection for USB OTG

2.2.1 IP3319CX6 - Product information

IP3319CX6 is an integrated common mode filter with ESD protection diodes. It is fabricated in a Wafer-Level Chip-Scale Package (WLCSP) offering a very high level of integration and smallest PCB area consumption. The integrated ESD protection diodes protect the two data lines and the ID pin against electrostatic discharge. Furthermore the integrated common mode filter provides a very good CMR for the differential data lines. Emission to the GSM-900 spectrum as well as for other wireless transmission standards (see marker (a) to (d) in Figure 3) are suppressed effectively. The pass band for the differential mode (S_{dd21})[1] is wide enough to allow a proper operation of the USB 2.0 interface.



(1) S_{dd21} differential mode

(2) S_{cc21} common mode

Potential interferer spectrum:

(a) GSM850/900; LTE

(b) GSM 1800/1900

(c) WIFI (2.4 GHz); LTE

(d) WIFI (5 GHz)

Fig 3. Differential mode and common mode insertion loss of IP3319CX6

2.2.2 IP3319CX6 - Application information

IP3319CX6 provides EMI filtering and ESD protection. For the common mode filtering it does not matter when the differential data lines D+ and D− are interchanged, as long as the proper electrical connection with the system chip is considered: In the application diagram (Figure 4) the signal path between solder balls A1 and A2 is connected to pin 2 of the Micro USB connector, as for balls B1 and B2 to pin 3. Depending on the actual placement of the components in a phone design it might result in crossed signal tracks. In that case the signal lines A and B of IP3319CX6 can be easily exchanged due to the symmetric architecture of the coil design.

1. For a detailed explanation of parameters S_{dd21} and S_{cc21} see Appendix 4.2.

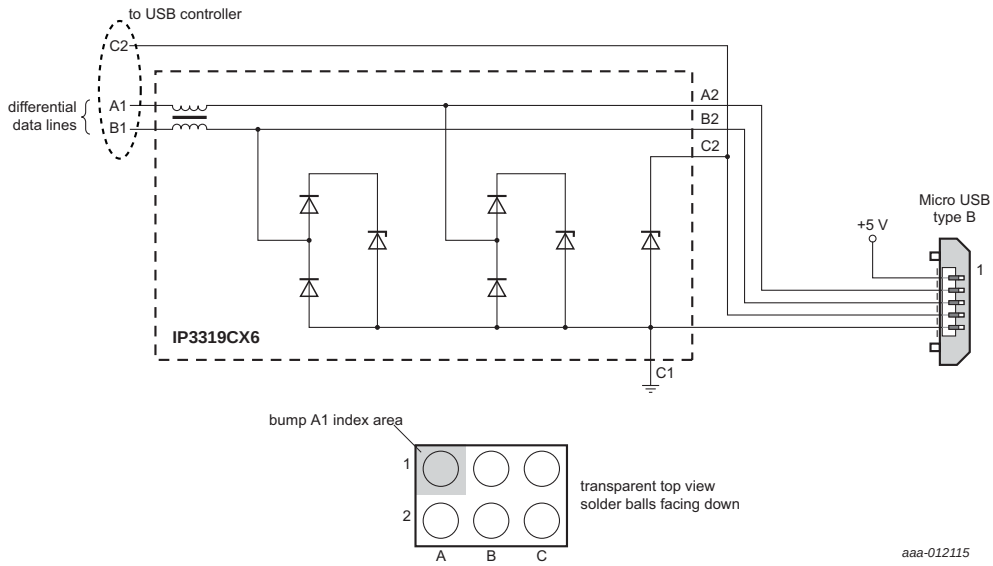


Fig 4. Typical application of IP3319CX6 at Micro USB connector in portable devices

2.2.3 IP3319CX6 - Layout recommendations

In order to provide best performance for the ESD protection a proper GND connection between the protection device and the USB connector is important. This connection should be short to minimize resistive and inductive impedance. A short connection is also essential for a short current return path towards GND of the connector during an ESD discharge event.

The pinning of IP3319CX6 is suited for the direct connection of a Micro USB connector. An exemplary layout is shown in Figure 5. The connection and routing of the differential data lines is straightforward. For best ESD protection the GND ball needs a direct connection with the GND/shield of the connector. In this example the GND ball C1 is connected by three vias to the GND layer of the PCB.

An alternative layout in Figure 6 uses a bottom or inner layer to connect the ID pin with the system chip. This layout allows a solid ground connection of the GND ball C1 in the top layer without additional layer changes.

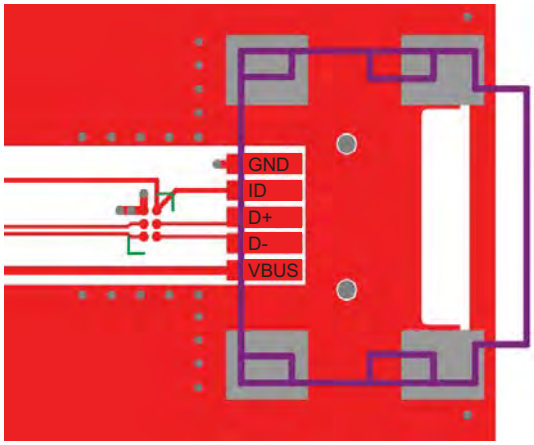


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Fig 5. Exemplary layout view for IP3319CX6 connected to a Micro USB connector

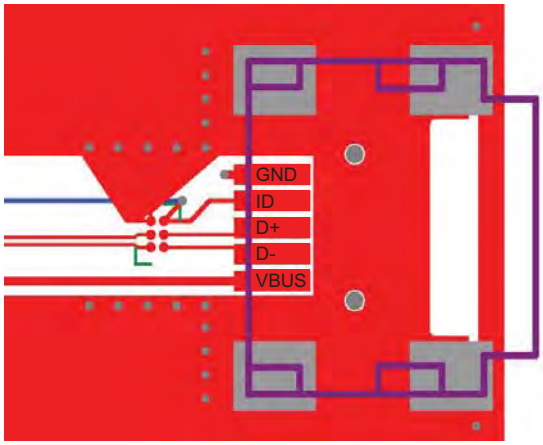

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Fig 6. Exemplary layout view for IP3319CX6 connected to a Micro USB connector, ID pin connected via bottom/inner layer

USB 2.0 eye diagram

The electrical specification of the USB 2.0 high-speed signaling mode states requirements for the eye patterns and rise and fall times. The template 5 names the most stringent limits with a minimum eye opening of ±300 mV measured at the plane TP4 as shown in Figure 7. In order to pass this test as shown in Figure 9 IP3319CX6 shows sufficient performance.

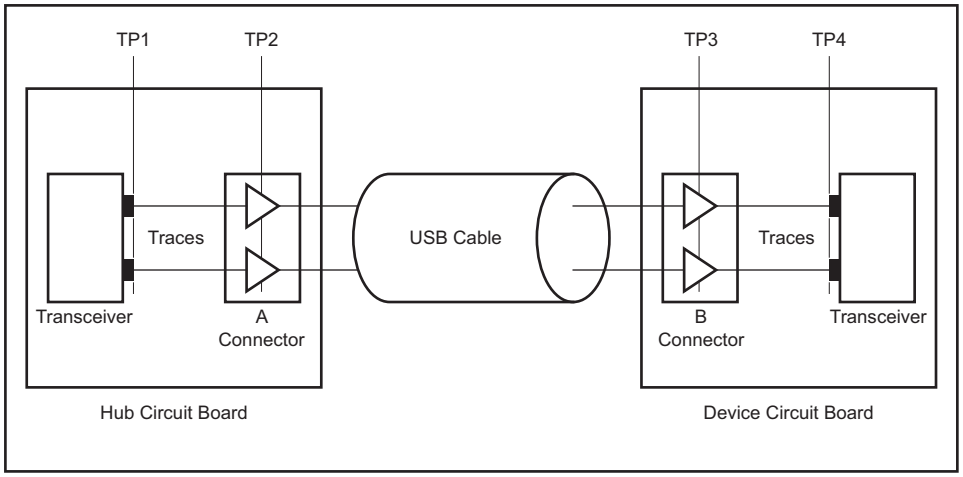


Fig 7. USB 2.0 - measurement planes in high-speed signaling mode

Table 1. Template 5

Transmit waveform requirements (Template 5) for device transceiver measured at TP4

Level	Voltage level (D+, D–)	Time (% of unit interval)
Level 1	+525 mV in UI following a transition; +475 mV in all others	n.a.
Level 2	–525 mV in UI following a transition; –475 mV in all others	n.a.
Point 1	0 V	5 %
Point 2	0 V	95 %
Point 3	+300 mV	35 %
Point 4	+300 mV	65 %
Point 5	–300 mV	35 %
Point 6	–300 mV	65 %

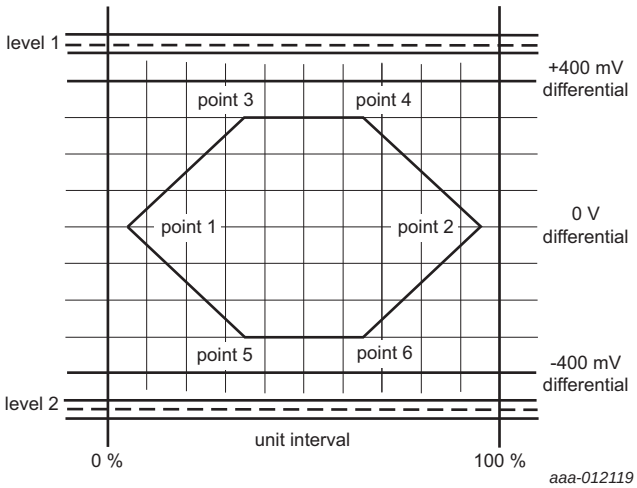


Fig 8. Transmit waveform requirements for device transceiver measured at TP4

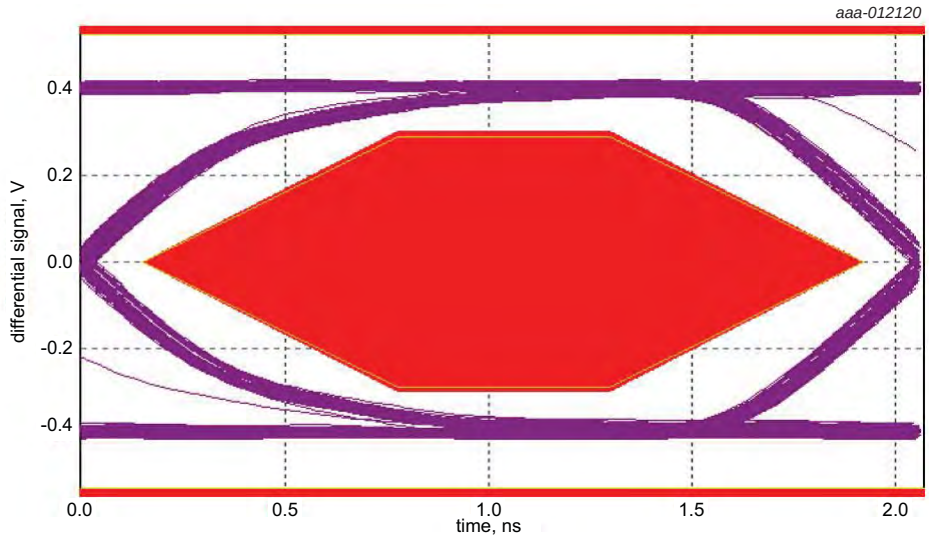


Fig 9. USB 2.0 eye diagram measured with IP3319CX6 at TP4 with 300 mV limits

3. Common Mode Filter for MIPI D-PHY interfaces

3.1 MIPI D-PHY interfaces in mobile phones

The MIPI[2] alliance has established standards for hardware and software interfaces in mobile devices. Among these interfaces in particular the camera and display interface – as used in modern smartphones – are the typical field of application for integrated common mode filters.

The D-PHY specification (Physical Layer Specification, 2013) defines a flexible, low-cost, high-speed serial interface for communication interconnections between components inside a mobile device. Traditionally, those interfaces used to be CMOS parallel buses at low bit rates with slow edges for EMI reasons. The D-PHY solution enables significant extension of the interface bandwidth for more advanced applications. Another benefit is their realization with very low-power consumption [mipi.org].

3.1.1 Display Serial Interface

The Display Serial Interface (DSI) specification defines protocols between a host processor and peripheral devices using a D-PHY physical interface. The DSI specification builds on existing specifications by adopting pixel formats and command sets defined in MIPI Alliance specifications for Display Pixel Interface 2 (DPI-2) and Display Command Set (DCS). The DSI specification defines a high-speed serial interface between a peripheral – such as an active-matrix display module – and a host processor in a mobile device [mipi.org].

2. MIPI is not an acronym and has no specific meaning (Frequently Asked Questions, 2013).

3.1.2 Camera Serial Interface CSI-2

Demand for increasingly higher image resolutions is pushing the bandwidth capacity of existing host processor-to-camera sensor interfaces. Common parallel interfaces are difficult to expand, require many interconnects and consume relatively large amounts of power. Emerging serial interfaces address many of the shortcomings of parallel interfaces while introducing their own problems. Incompatible, proprietary interfaces prevent devices from different manufacturers from working together. Results are raising system costs and reduction of system reliability, what requires 'hacks' to force the devices to inter-operate. CSI-2 provides the mobile industry a standard, robust, scalable, low-power, high-speed, cost-effective interface that supports a wide range of imaging solutions for mobile devices [mipi.org].

The Camera Serial Interface 2 specification defines an interface between a peripheral device (camera) and a host processor (baseband, application engine). The purpose of this specification is to identify a standard interface between a camera and a host processor for mobile device applications. This data transmission interface (referred as CSI-2) is a unidirectional differential serial interface with data and clock signals.The physical layer of this interface is the MIPI Alliance Standard for D-PHY (Physical Layer Specifications, 2013).

3.1.3 MIPI D-PHY application

Figure 10 illustrates a connection between CSI-2 transmitter and receiver, which typically are a camera module and the system chip as components in a mobile phone. As shown in this application diagram one differential lane is used to transmit the clock signal. At least one differential lane is used for data transmission. Cameras with high-resolution sensors have up to four differential data lanes. Depending on the number of total lanes either filter devices with two or three channels can be used in combination to provide sufficient common mode rejection in the mobile phone application. The suppression of common mode signals significantly helps to avoid sensitivity issues for the integrated receiver modules in smartphones (GSM, 3G, LTE, GPS or also WIFI in the 2.4 GHz and 5 GHz bands) in particular during operation of the camera module.

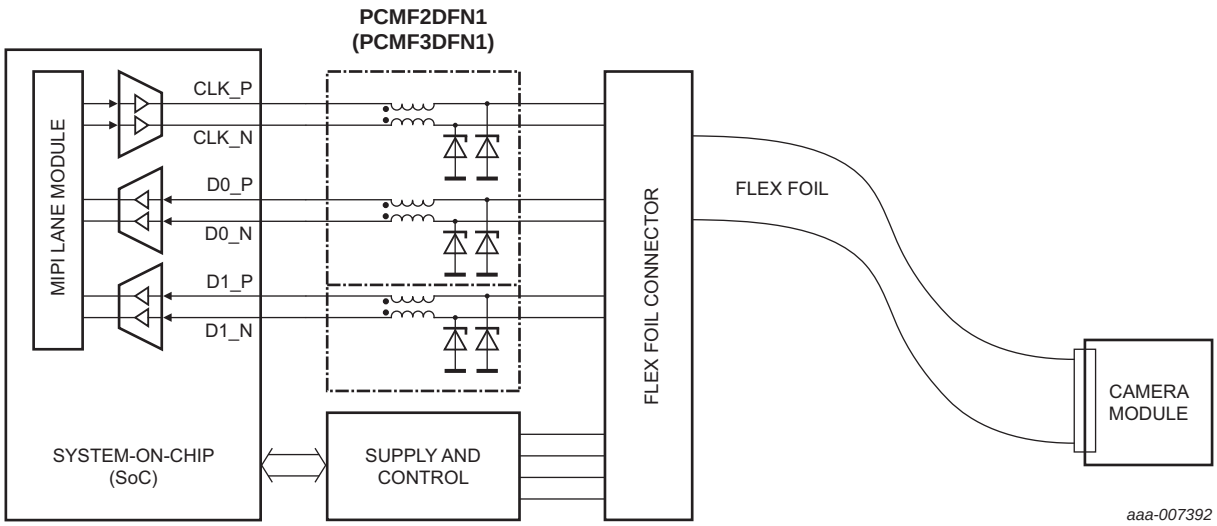


Fig 10. Application diagram for MIPI CSI: Two/three channel interface, using either PCMF2DFN1 or PCMF3DFN1

Figure 11 depicts the connection between display and system chip. Here both – clock and data lines – are driven by the system chip and connected to D-PHY receiver ports at the display controller inside the display module. While Figure 11 shows four differential data lanes other applications might use only two or three.

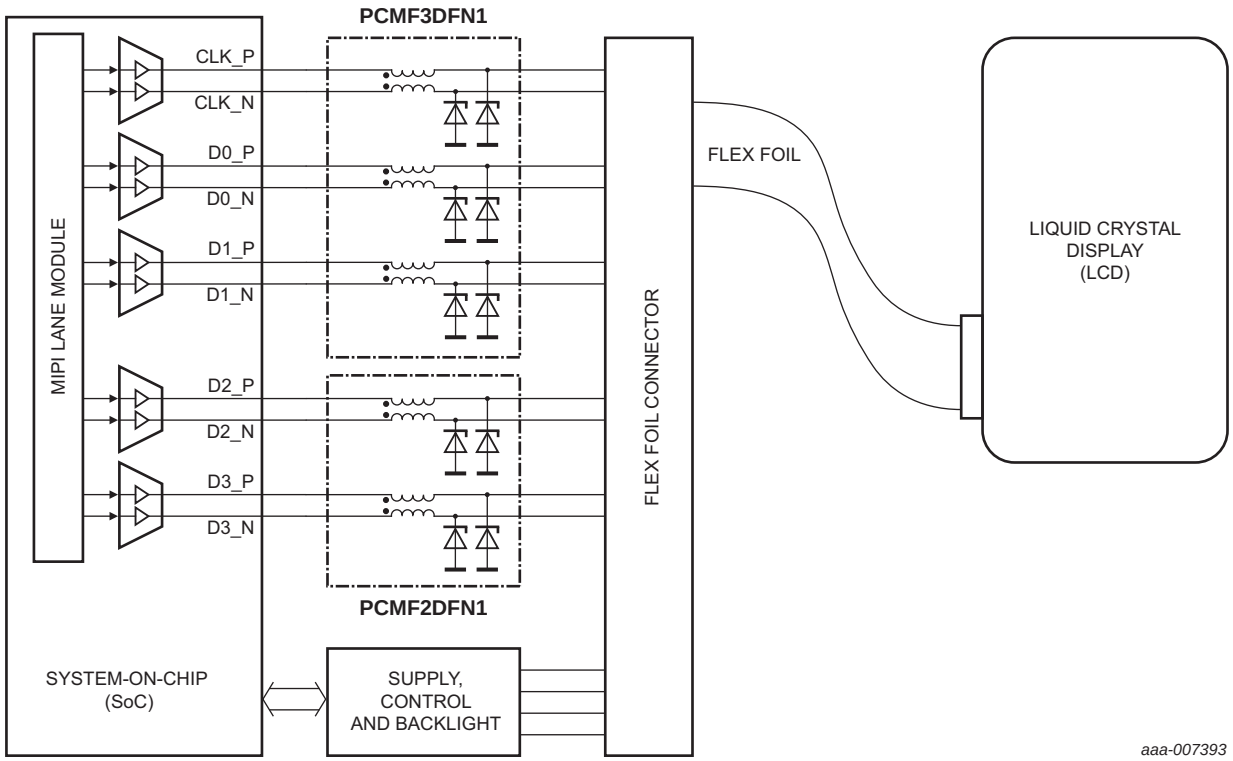


Fig 11. Application diagram for MIPI DSI: Five channel interface, using PCMF2DFN1 together with PCMF3DFN1

Depending on the actual display or sensor size, resolution and repetition rate of the image data, the total number of data lines and the actual clock and data frequency can be adjusted only within certain limits. Considering the spectral power density of MIPI clock and data signals there can be significant energy present in the same spectrum as used by GSM, WIFI (2.4 GHz and 5 GHz), GPS or LTE radio modules. In theory the differential signal lines show little tendency to radiate. Any imbalance in the MIPI transmitter, signal routing or connectors results in conversion from differential to common mode signals. These common mode signals are very likely to radiate and affect the aforementioned receiver modules which are only few millimeters or centimeters apart.

Here a common mode filter with high suppression for the common mode in the receiving frequency bands will help to avoid receiver sensitivity degradation during the operation of the camera or display interface. Figure 12 and Figure 13 show the spectral power density in logarithmic amplitude scale for a MIPI data and clock signal with 130 MS/s. While the fundamental spectrum is far below any sensitive receiving frequency the odd multiples (3 ×, 5 ×, 7 ×, …) show still significant energy which could result in unwanted interferences. The common mode filter must not change the differential signal as it would degrade the signal integrity in the time domain (visible in the opening of the eye-diagram).

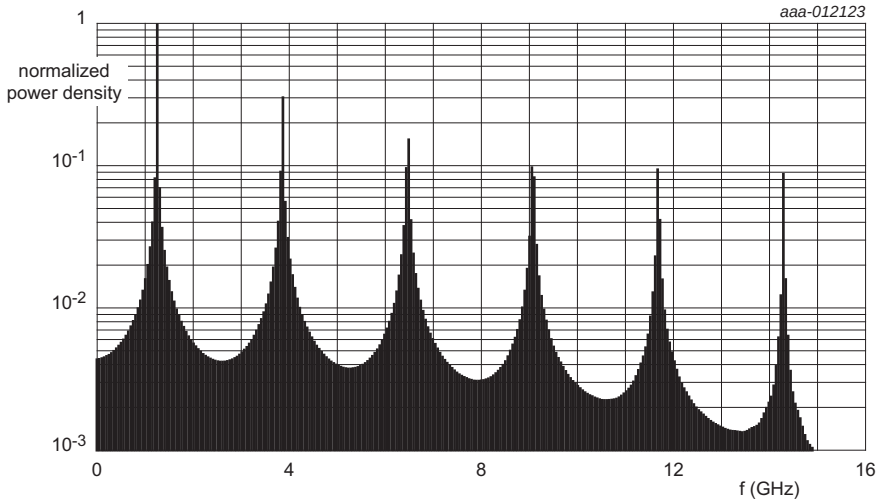


Fig 12. MIPI D-PHY: Example of spectral power density of differential clock line

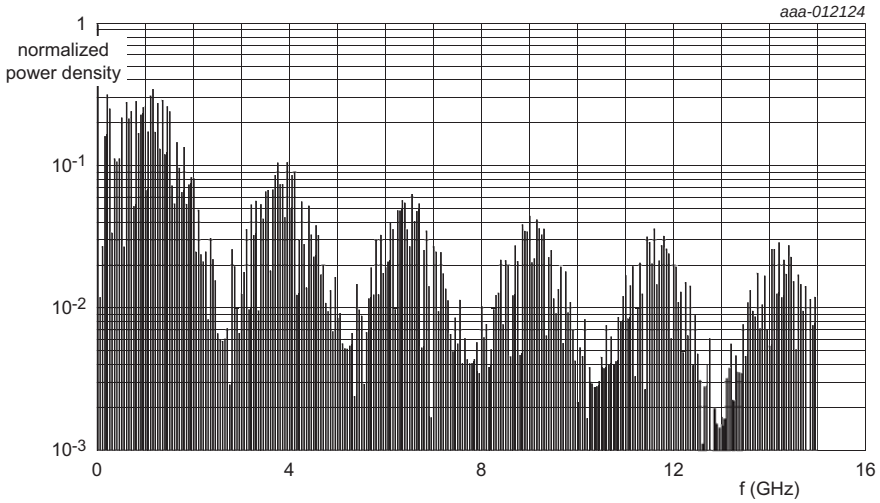


Fig 13. MIPI D-PHY: Example of spectral power density of differential data line

3.2 PCMF2DFN1, PCMF3DFN1 – Two and Three Channel Common Mode Filters with integrated ESD protection

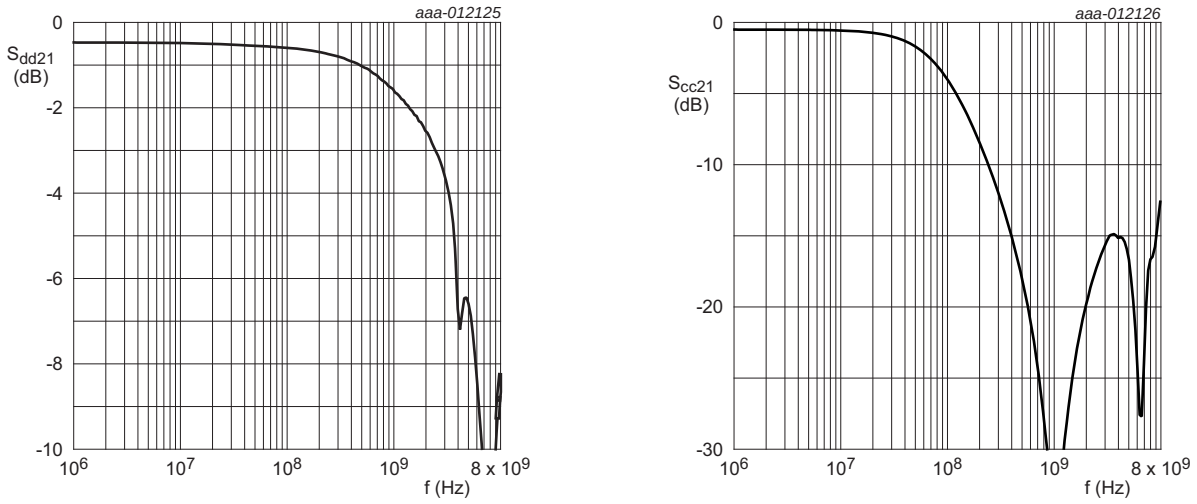
3.2.1 PCMFxDFN1 – Product information

The devices of the PCMFxDFN1 family provide EMI filtering and ESD protection for high-speed differential signal lines. Key applications are Camera and Display Serial interfaces based on MIPI D-PHY as they are widely used in Tablet PCs and smartphones.

PCMF2DFN1 protects two channels and is housed in a 2.5 mm × 2.0 mm DFN2520-9 (SOT1333-1) plastic package.

PCMF3DFN1 protects three differential channels and is housed in a 4.0 mm × 2.0 mm DFN4020-14 (SOT1334-1) plastic package.

Both packages offer a maximum height of 0.5 mm following the requirements of low profile packages in current mobile phone designs.



a. S_{dd21} - Differential mode insertion loss

b. S_{cc21} - Common mode insertion loss

Fig 14. Differential and common mode insertion loss for one different channel

3.2.2 PCMFxDFN1 – EMI filtering and ESD protection

The fundamental electric characteristic of common mode filters is the frequency response in differential and common mode operation as shown in Figure 14.

The −3 dB cut-off frequency for the differential pass band is above 2.2 GHz and allows passing the wanted clock or data signal without significant impact on the signal integrity, i.e. the eye diagram remains open.

The frequency characteristic of the common mode signal shows a deep notch at the GSM-900 band. This reduces unwanted radiation of the D-PHY lines into the integrated antennas of the mobile phone by more than 25 dB. Another benefit of PCMFxDFN1 common mode rejection is the attenuation in the spectrum above 2 GHz which is typically higher than 15 dB. Most ferrite-based common mode filters do not reach this strong CM attenuation and cause potential EMI issues for integrated WIFI (2.4 GHz, 5 GHz), GPS and LTE receivers. In a direct comparison, all of the measured ferrite based common mode filters have less CMR in the GSM spectrum and show very poor common mode suppression in the upper frequency spectrum above 1 GHz (see Figure 15).

In a typical camera application as used in mobile phones an electrostatic discharge can occur through the gap around the camera lens and finally hit the sensitive camera module or the connection made on flex foil PCB. The integrated ESD protection diodes of the PCMFxDFN1 devices provide protection against damage by ESD pulses. The diodes are placed on one side of the filter. For optimum ESD protection it is important to connect this side of the filter towards the display or camera connector as shown in Figure 11.

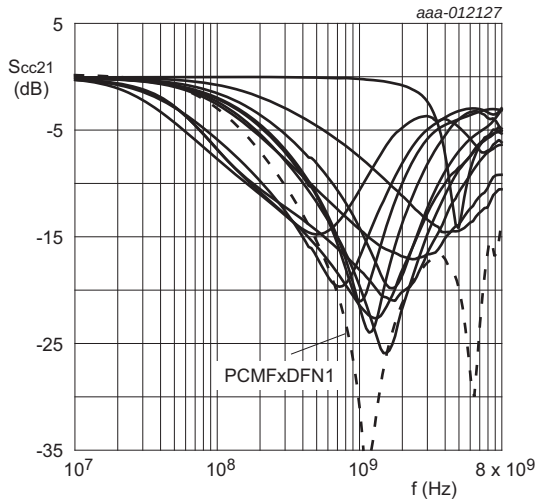


Fig 15. Common mode frequency response (S_{cc21}) of PCMFxDFN1 compared to various ferrite-based common mode filters

3.2.3 PCMFxDFN1 – Layout recommendations

An exemplary layout view for PCMFxDFN1 in MIPI interface applications is shown in Figure 16 below. Following recommendations result in best performances for the filter characteristic and ESD protection:

- Solid ground connection (by multiple vias to the GND layer) placing vias close to the GND-pins of PCMFxDFN1
- Same PCB trace length for positive and negative signal lines of each differential channel
- Design of PCB trace width and spacing according to the characteristic impedance (for example 100 Ω for MIPI, 90 Ω for USB)
- Avoiding multiple layer changes for signal lines, unless needed for shielding and connection reasons

In the layout example the differential signal lines are routed on an inner layer between system chip and PCMFxDFN1. Next to the common mode filter the connection to the pins are made by vias. Using blind vias can reduce unwanted interference from the opposing PCB side. The approach with signal lines on inner layers allows separate shield encasing for the SoC on the one hand and the common mode filter combined with flex foil connector on the other hand.

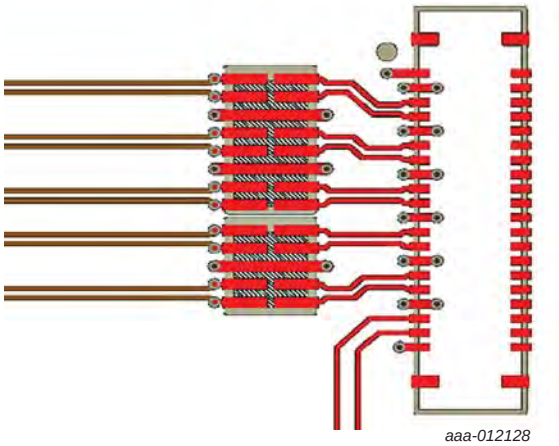


Fig 16. 5-channel MIPI interface: Exemplary layout view for PCMF2DFN1 and PCMF3DFN1 connected to a flex foil connector

4. Appendix

The most important parameters to characterize common mode filters are the scattering parameters (S-parameters) S_{dd21} for differential mode and S_{cc21} for common mode operation. The following paragraphs provide a brief introduction into general scattering parameters as well as the so called mixed-mode S-parameters.

4.1 Introduction into general S-parameters

Scattering parameters (also called S-parameters) describe the electrical behavior of linear electrical networks. They are commonly used to characterize networks at higher frequencies since other parameters (for example Z-parameters) require the measurement of voltage and current – which can be difficult or even impossible at higher frequencies.

The term 'scattering' is derived from optical phenomena where light – as a representation of electromagnetic waves – is scattered, reflected and transmitted at the boundary of different materials.

Looking in general at a Device Under Test (DUT) with two (coaxial) inputs this DUT can be considered as a two-port device. At each port an incident electromagnetic wave moving towards the port is denoted by the letter a and corresponding indices 1 and 2. In the same manner, waves moving away from the port are denoted by letter b.

The wave b_1 is composed from the transmitted part of wave a_2 travelling towards port 2 and a fraction of wave a_1 that is reflected at port 1. In same manner b_2 is added by reflected fraction of wave a_2 and transmitted part of wave a_1.

These two equations show both:

$$b_1 = S_{11} \times a_1 + S_{12} \times a_2 \quad (1)$$

$$b_2 = S_{21} \times a_1 + S_{22} \times a_2 \quad (2)$$

Here S_{11} and S_{22} represent the reflection coefficient at each port:

- $S_{11} = b_1/a_1$ with $a_2 = 0$ (i.e. no incident wave a_2 at port 2)
- $S_{22} = b_2/a_2$ with $a_1 = 0$ (i.e. no incident wave a_1 at port 1)

The transmission from one port to another:

- $S_{12} = b_1/a_2$ with $a_1 = 0$ (i.e. perfect termination of port 1)
- $S_{21} = b_2/a_1$ with $a_2 = 0$ (i.e. perfect termination of port 2)

The two equations Equation 1 and Equation 2 can also be written in matrix representation:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \quad (3)$$

$$b = S \cdot a \quad (4)$$

The matrix **S** represents the scattering matrix of a two-port device. Each element is a complex number (i.e. is composed of real and imaginary part or magnitude and phase) and typically varies with frequency. The measurement of S is done with Vector Network Analyzers (VNA) which allow measurements of magnitude and phase of each S-parameter over a wide frequency range.

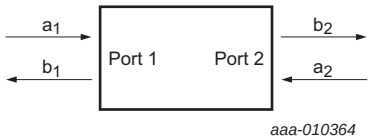


Fig 17. Two-port device with incident and outgoing waves

The extension from a two-port device to a four-port device is straight forward: The DUT and the VNA have both four single-ended (coaxial) ports. The corresponding scattering matrix **S** holds 16 elements representing all possible coupling paths between the four ports:

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{bmatrix} \cdot \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{bmatrix} \quad (5)$$

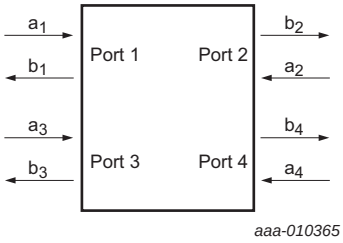


Fig 18. Four-port device with incident and outgoing waves

4.2 Mixed-mode S-parameters

The four physical ports of a DUT as shown in Figure 16 can be considered as two logical ports that are operated in a differential mode, typically the wanted mode of operation for differential signal lines in high-speed differential interfaces (USB, SATA, PCIe, …). Furthermore another mode which is related to the common ground reference can occur: the common mode, in most applications this is an unwanted mode since it is strongly linked to EMI issues like radiation or susceptibility to external electromagnetic fields. During the operation in differential and/or common mode the four physical ports are seen as two logical ports. For the characterization of this two-port device the mixed-mode S-parameters can be used. At each logical port a differential wave can travel towards the port (a_{d1} and a_{d2} as well as outgoing waves b_{d1}, b_{d2} can occur. Just looking on this differential mode the matrix **SD** allows to characterize this two-port:

$$\begin{bmatrix} b_{d1} \\ b_{d2} \end{bmatrix} = \begin{bmatrix} S_{dd11} & S_{dd12} \\ S_{dd21} & S_{dd22} \end{bmatrix} \begin{bmatrix} a_{d1} \\ a_{d2} \end{bmatrix} \tag{6}$$

In the same way the common mode response can be given by a single matrix with four elements:

$$\begin{bmatrix} b_{c1} \\ b_{c2} \end{bmatrix} = \begin{bmatrix} S_{cc11} & S_{cc12} \\ S_{cc21} & S_{cc22} \end{bmatrix} \begin{bmatrix} a_{c1} \\ a_{c2} \end{bmatrix} \tag{7}$$

Furthermore a mode-conversion might occur where an incident differential wave a_{d1} is converted into an outgoing common mode wave b_{c2}. Taking all possible conversion schemes and the above noted equations for pure differential and common mode into account this full mixed-mode S-parameter matrix can be used to describe this DUT:

$$\begin{bmatrix} b_{d1} \\ b_{d2} \\ b_{c1} \\ b_{c2} \end{bmatrix} = \begin{bmatrix} \begin{bmatrix} S_{dd11} & S_{dd12} \\ S_{dd21} & S_{dd22} \end{bmatrix} & \begin{bmatrix} S_{dc11} & S_{dc12} \\ S_{dc21} & S_{dc22} \end{bmatrix} \\ \begin{bmatrix} S_{cd11} & S_{cd12} \\ S_{cd21} & S_{cd22} \end{bmatrix} & \begin{bmatrix} S_{cc11} & S_{cc12} \\ S_{cc21} & S_{cc22} \end{bmatrix} \end{bmatrix} \begin{bmatrix} a_{d1} \\ a_{d2} \\ a_{c1} \\ a_{c2} \end{bmatrix} \tag{8}$$

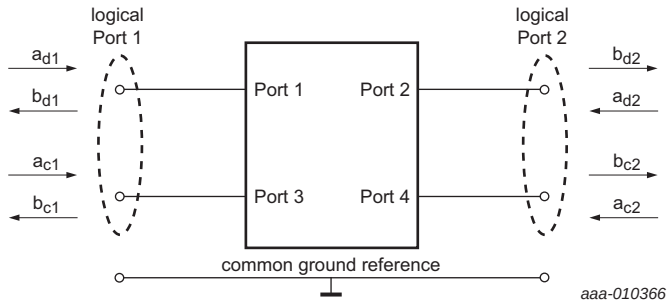


Fig 19. Two-port device (made by four physical ports) in differential and common mode operation

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